Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 21. (canceled)

Claim 22. (Currently Amended) An apparatus for executing a Viterbi algorithm, comprising:

initial state registers each storing a state metric of an initial state of a trellis having a butterfly structure, a state metric, and a transition metric;

at least one transition register storing the transition metric of the trellis;

evaluation units;

an adder/subtracter network for processing signals, said adder/subtracter network connected:

to said initial state registers;

to said at least one transition register; and

to said evaluation units in accordance with the butterfly structure of the trellis;

said evaluation units evaluating signals processed by said

adder/subtracter network in accordance with a Viterbi algorithm;

a selection unit switching the apparatus between a first operating mode and a second operating ~~modes~~ mode, wherein the first operating mode is in a different field of operation than the second operating mode;

final state registers connected to said evaluation units, each of said final state registers storing the state metric of a respective final state of the trellis; and

said selection unit selecting different ones of said evaluation units in dependence upon a selected one of said first and second operating modes.

Claim 23. (Previously Presented) The apparatus according to claim 22, wherein at least one of said initial state registers has a buffer register.

Claim 24. (Previously Presented) The apparatus according to claim 22, wherein said at least one transition register at least one of:

stores a transition metric when said selection unit switches the apparatus to said first operating mode; and

stores a change transition metric when said selection unit

switches the apparatus to said second operating mode.

Claim 25. (Previously Presented) The apparatus according to claim 22, wherein said at least one transition register:

stores a transition metric when said selection unit switches the apparatus to said first operating mode; and

stores a change transition metric when said selection unit switches the apparatus to said second operating mode.

Claim 26. (Previously Presented) The apparatus according to claim 22, wherein said at least one transition register is at least two transition registers storing two different transition metrics when said selection unit switches the apparatus to said second operating mode.

Claim 27. (Previously Presented) The apparatus according to claim 22, including:

a signal bus connected to said initial state registers, said at least one transition register, and said final state registers; and

a processor connected to said initial state registers, said at least one transition register, and said final state registers through said signal bus.

Claim 28. (Previously Presented) The apparatus according to claim 27, wherein said processor is programmed to calculate the state metric and the transition metric.

Claim 29. (Previously Presented) The apparatus according to claim 22, including:

a signal bus connected to said initial state registers, said at least one transition register, and said final state registers; and

a memory connected to said initial state registers, said at least one transition register, and said final state registers through said signal bus, said memory storing the state metric and the transition metric.

Claim 30. (Previously Presented) The apparatus according to claim 27, including a memory connected to said initial state registers, said at least one transition register, and said final state registers through said signal bus, said memory storing the state metric and the transition metric.

Claim 31. (Previously Presented) The apparatus according to claim 22, wherein said adder/subtracter network includes at least one of:

an adder; and

a subtracter.

Claim 32. (Previously Presented) The apparatus according to claim 22, wherein:

said at least one of said initial state registers includes a first initial state register and a second initial state register;

said first initial state register has a first buffer register with a first buffer register output;

said second initial state register has a second buffer register with a second buffer register output;

said adder/subtracter network includes three adders and three subtracters;

each of said three adders and said three subtracters has a first input, a second input, and an output;

said at least one transition register includes a first transition register, a second transition register, and a third transition register;

said first transition register has a first transition register output;

said second transition register has a second transition register output;

said third transition register has a third transition register output;

said first input of said first adder is connected to said first transition register output;

said second input of said first adder is connected to said second transition register output;

said first input of said first subtracter is connected to said second transition register output;

said second input of said first subtracter is connected to said third transition register output;

said first input of said second adder is connected to said first buffer register output;

said second input of said second adder is connected to said output of said first adder;

said first input of said second subtracter is connected to said first buffer register output;

said second input of said second subtracter is connected to said output of said first adder;

said first input of said third adder is connected to said output of said first subtracter;

said second input of said third adder is connected to said second buffer register output;

said first input of said third subtracter is connected to said output of said first subtracter; and

said second input of said third subtracter is connected to said second buffer register output.

Claim 33. (Previously Presented) The apparatus according to claim 22, wherein said evaluation units include at least one of:

a trace-back register;

comparison units; and

maximum selection elements.

Claim 34. (Previously Presented) The apparatus according to claim 33, wherein:

said trace-back register has a control input, a first data input, and a second data input;

said final state registers include a first final state

register with a control output;

said control input of said trace-back register is connected to said control output of said first final state register such that, when a value is read from said first final state register, said trace-back register can store new values;

said comparison units include:

a first comparator with a first comparator output; and

a second comparator with a second comparator output;

said first comparator output is connected to said first data input of said trace-back register, and

said second comparator output is connected to said second data input of the trace-back register.

Claim 35. (Previously Presented) The apparatus according to claim 32, wherein said evaluation units include at least one of:

a trace-back register;

comparison units including:

a first comparator with a first comparator output, a first input, and a second input; and

a second comparator with a second comparator output, a first input, and a second input;

maximum selection elements;

said first input of said first comparator is connected to said output of said second adder;

said second input of said first comparator is connected to said output of said third subtracter;

said first input of said second comparator is connected to said output of said second subtracter; and

said second input of said second comparator is connected to said output of said third adder.

Claim 36. (Previously Presented) The apparatus according to claim 32, wherein:

said trace-back register has a control input, a first data input, and a second data input;

said final state registers include a first final state register with a control output;

said control input of said trace-back register is connected to said control output of said first final state register such that, when a value is read from said first final state

register, said trace-back register can store new values;

comparison units including:

a first comparator with a first comparator output, a first input, and a second input; and

a second comparator with a second comparator output, a first input, and a second input;

said first comparator output is connected to said first data input of said trace-back register;

said second comparator output is connected to said second data input of the trace-back register;

said first input of said first comparator is connected to said output of said second adder;

said second input of said first comparator is connected to said output of said third subtracter;

said first input of said second comparator is connected to said output of said second subtracter; and

said second input of said second comparator is connected to said output of said third adder.

Claim 37. (Previously Presented) The apparatus according to claim 35, wherein:

said maximum selection elements include:

a first maximum selection element having a control input, a first input, and a second input;

a second maximum selection element having a control input, a first input, and a second input;

said final state registers include a second final state register with a control output;

said control input of said first maximum selection element is connected to said control output of said first final state register such that, when a value is read from said first final state register, said first maximum selection element can select a new value;

said first input of said first maximum selection element is connected to said output of said second adder;

said second input of the first maximum selection element is connected to said output of said second subtracter;

said control input of said second maximum selection element is connected to said control output of said second final state register such that, when a value is read from said second final state register, said second maximum selection element

can select a new value;

said first input of said second maximum selection element is connected to said output of said third subtracter; and

said second input of said second maximum selection element is connected to said output of said third adder.

Claim 38. (Previously Presented) The apparatus according to claim 36, wherein:

said maximum selection elements include:

a first maximum selection element having a control input, a first input, and a second input;

a second maximum selection element having a control input, a first input, and a second input;

said final state registers include a second final state register with a control output;

said control input of said first maximum selection element is connected to said control output of said first final state register such that, when a value is read from said first final state register, said first maximum selection element can select a new value;

said first input of said first maximum selection element is connected to said output of said second adder;

said second input of the first maximum selection element is connected to said output of said second subtracter;

said control input of said second maximum selection element is connected to said control output of said second final state register such that, when a value is read from said second final state register, said second maximum selection element can select a new value;

said first input of said second maximum selection element is connected to said output of said third subtracter; and

said second input of said second maximum selection element is connected to said output of said third adder.

Claim 39. (Previously Presented) The apparatus according to claim 22, wherein said selection unit includes a selection register and at least one multiplexer is connected to said selection unit.

Claim 40. (Previously Presented) The apparatus according to claim 32, wherein said selection unit includes a selection register and at least one multiplexer is connected to said selection unit.

Claim 41. (Previously Presented) The apparatus according to claim 40, wherein:

a signal bus is connected to said initial state registers, said at least one transition register, and said final state registers;

said at least one multiplexer includes:

a first multiplexer having:

a control input;

a first data input; and

a second data input;

a second multiplexer having:

a control input;

a first data input; and

a second data input;

a third multiplexer having:

a control input;

a first data input; and

a second data input;

said evaluation units include:

a trace-back register with a first data output, a first data input, and a second data output;

comparison units; and

maximum selection elements including a first maximum selection element with an output;

said selection register has an input connected to said signal bus and an output connected to said control input of said first multiplexer;

said first data input of said first multiplexer is connected to said first data output of said trace-back register;

said second data input of said first multiplexer is connected to said output of said first maximum selection element;

said control input of said second multiplexer is connected to said first data input of said trace-back register;

said first data input of said second multiplexer is connected to said output of said second adder;

said second data input of said second multiplexer is connected

to said output of said third subtracter;

said comparison units include:

a first comparator; and

a second comparator with a second comparator output

said control input of said third multiplexer is connected to said second comparator output;

said first data input of said third multiplexer is connected to said output of said second subtracter; and

said second data input of said third multiplexer is connected to said output of said third adder.

Claim 42. (Previously Presented) The apparatus according to claim 22, wherein said first operating mode is a mode in which decoding is carried out in accordance with the Viterbi algorithm.

Claim 43. (Previously Presented) The apparatus according to claim 22, wherein said second operating mode is a mode in which equalization is carried out in accordance with the Viterbi algorithm.

Claim 44. (Currently Amended) A method for executing a

Viterbi algorithm, which comprises:

selecting one of ~~two operating modes~~ a first operating mode and a second operating mode of an apparatus to execute the Viterbi algorithm, wherein the first operating mode is in a different field of operation than the second operation mode;

respectively storing a state metric of an initial state of a trellis in an initial state register;

storing at least one transition metric of the trellis dependent upon on the selected one of the operating modes;

linking the state metrics of the initial states and the transition metric to one another according to a butterfly structure of the trellis using the Viterbi algorithm dependent upon the selected one of the operating modes;

selecting linked variables dependent upon the selected one of the operating modes;

storing the selected linked variables as state metrics of a respective final state of the trellis; and

iteratively carrying out the preceding steps of the method until the Viterbi algorithm ends.

Claim 45. (Previously Presented) The method according to claim 44, which further comprises using the Viterbi algorithm

to process physical signals.

Claim 46. (Previously Presented) The method according to claim 44, which further comprises using the Viterbi algorithm to equalize and decode received

physical signals dependent upon the selected one of the operating modes.

Claim 47. (Previously Presented) The method according to claim 44, which further comprises using the Viterbi algorithm to decode received physical signals in a first of the operating modes and to equalize the received physical signals in a second of the operating modes.

Claim 48. (Previously Presented) The method according to claim 44, which further comprises:

decoding physical signals in a first of the operating modes; and

equalizing the physical signals in a second of the operating modes.

Claim 49. (Previously Presented) The method according to claim 44, which further comprises:

storing a respective state metric, which is stored in the initial state register, of the initial state of the trellis in a respective buffer register as soon as a final state has been read from a final state register; and

storing a new state metric of the initial state of the trellis in a respective initial state register as soon as the respective initial state of the trellis has been stored in the buffer register.